PCB DESIGN REVIEW

PCB Design Review Checklist

2026 Edition

E-Sharp AB
esharp.se

BEFORE YOU OPEN THE SCHEMATIC

- [ ] **Requirements**
  Spec exists; the design's scope matches it
- [ ] **Interfaces**
  Levels, protocol, connector, pinout, mating part
- [ ] **Constraints**
  Size, cost, thermal, regulatory, mandated parts

POWER

- [ ] **Rails**
  V, tolerance, worst-case current; sized w/ margin
- [ ] **Sequencing**
  Power-up/down order; enables; supervisors
- [ ] **Derating**
  Within V/I/thermal limits; rating in the BOM
- [ ] **Decoupling**
  Per datasheet; bulk + local; short return path

CONNECTIVITY

- [ ] **Pin assignments**
  Right net; swappable pins chosen deliberately
- [ ] **Net naming**
  Consistent, meaningful; no default names left
- [ ] **Signal direction**
  Driven once; no floats; pulls where needed

COMPONENT

- [ ] **Availability**
  Sourceable now; 2nd source for critical parts
- [ ] **Ratings**
  Meet worst case; right package + temp grade
- [ ] **Lifecycle**
  Nothing NRND/EOL without a plan

LAYOUT

- [ ] **Return paths**
  Continuous reference plane; no split crossed
- [ ] **Clearances**
  Creepage/clearance; mfg spacing; keepouts
- [ ] **Critical nets**
  Length/impedance to spec; diff pairs matched

MANUFACTURING

- [ ] **Assembly**
  Footprints to datasheet; pin-1/polarity; fiducials
- [ ] **Testability**
  Test points; programming/JTAG access; test plan

DOCUMENTATION

- [ ] **Deliverables**
  Schematic, BOM (ratings+sources), fab + ODB++
- [ ] **Decisions**
  Non-obvious choices + waivers written down

A checklist isn't a review

A ticked box is a claim, not proof. The list tells you what to check — it doesn't verify. Record findings against the design, with evidence, and keep them for the next board.

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